

**United States Court of Appeals
for the Federal Circuit**

GENUINE ENABLING TECHNOLOGY LLC,
Plaintiff-Appellant

v.

**SONY GROUP CORPORATION, SONY
INTERACTIVE ENTERTAINMENT LLC,**
Defendants-Appellees

2024-1686

Appeal from the United States District Court for the
District of Delaware in No. 1:17-cv-00135-MSG, Judge
Mitchell S. Goldberg.

Decided: February 19, 2026

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Also represented by MICHELLE DAWSON, ERIN DUNGAN,
BRITTA LOFTUS, PAUL J. ROBBENNOLT.

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sented by CLIFFORD T. BRAZEN, ADAM PRESCOTT SEITZ,
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Before DYK, TARANTO, and CHEN, *Circuit Judges*.

CHEN, *Circuit Judge*.

Genuine Enabling Technology LLC (GET) appeals the U.S. District Court for the District of Delaware’s grant of summary judgment of noninfringement in favor of Sony Group Corporation & Sony Interactive Entertainment LLC (collectively, Sony). *Genuine Enabling Tech. LLC v. Sony Corp.*, No. 17-CV-135, 2024 WL 1255513, at *1 (D. Del. Mar. 25, 2024) (*Decision*). The district court determined that GET raised no genuine issue of material fact as to whether Sony’s Accused Products—PlayStation 3 and 4 controllers and consoles—infringe claims 10, 14, 16–18, and 21–23 of U.S. Patent No. 6,219,730 (’730 patent). *Id.* GET also appeals the district court’s exclusion of testimony from its expert, Dr. Fernald. *Genuine Enabling Tech. LLC v. Sony Corp.*, No. 17-CV-135, 2022 WL 17325656, at *8 (D. Del. Nov. 28, 2022) (*Daubert Order*). The key claim limitation in this dispute is a means-plus-function limitation—“encoding means for synchronizing” two input data streams—and the specification describes FIG. 4A’s logic block 34, a logic design circuit containing a multitude of elements, as the corresponding structure for performing the synchronizing function. Because GET and its expert failed to account for many of the elements in block 34 in their infringement analysis, we agree with the district court that GET presented a deficient infringement case as to this limitation and we thus *affirm*.

BACKGROUND

I

The ’730 patent generally relates to input devices for a computer. At the time of invention, there were several options for user-input devices for a computer including a keyboard, mouse, or pen-based input device. Additional input data could come from sources like a microphone or modem. In order to receive data from these sources, a computer

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needed dedicated resources for each input device (e.g., their own port), which created problems due to limited resources. *See* '730 patent col. 1 ll. 24–29. The '730 patent discloses a solution to the limited resources problem: combining the data streams from different input devices to minimize the number of computer resources. *Id.* col. 1 ll. 47–51.

Dependent claim 10 is representative¹ and states:

A user input apparatus operatively coupled to a computer via a communication means additionally receiving at least one input signal, comprising:

user input means for producing a user input stream;

input means for producing the at least one input signal;

converting means for receiving the at least one input signal and producing therefrom an input stream; and

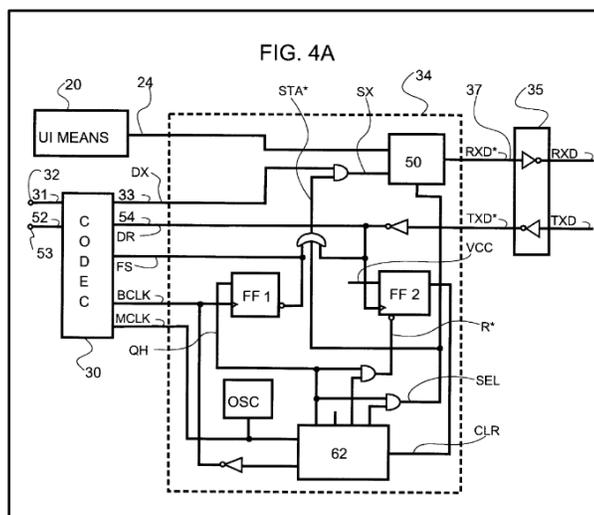
encoding means for synchronizing the user input stream with the input stream and encoding the same into a combined data stream transferable by the communication means,

wherein the input means is an input transducer.

Id. col. 8 ll. 26–27; *id.* col. 7 l. 61 – col. 8 l. 4 (emphasis added).

¹ Claim 10 is a dependent claim that depends from claim 1. The reproduction here incorporates the limitations of claim 1 into claim 10.

Each of claims 10, 14, 16–18, and 21–23 (Asserted Claims) includes an “encoding means”² limitation, emphasized above. The ’730 patent specification states that the claimed structure “keeps [user input] stream 24 and input stream 33 in synchrony and encodes^[3] them into [a] combined data stream 37 in accordance with the protocol of the communication means.” *Id.* col. 4 ll. 12–15 (cleaned up).



Id., FIG. 4A.

The ’730 patent discloses a representative embodiment of the “encoding means” (also referred to as a “framer”):

² Terms used in the Asserted Claims include “encoding means,” “framer,” and “means for synchronizing and encoding.” Both parties agree these terms refer to the same means-plus-function limitation, and the district court gave them all the same construction. *See* Appellant Br. 6–7; Appellee Br. 14 n.1; *Decision*, 2024 WL 1255513, at *1. For simplicity, we refer to all versions as the “encoding means” limitations.

³ We focus on the synchronize function in this opinion because, as the district court noted, it “best illustrates” the issues. *See Daubert Order*, 2022 WL 17325656, at *3.

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logic block 34 in FIG. 4A as depicted above. *See id.* col. 5 ll. 4–6. Several components of logic block 34 are depicted as boxes including data selector 50, clock generator 62, and oscillator OSC. *Id.* col. 5 ll. 47–50, 59–62.

The specification includes a detailed description of block 34’s multi-step synchronization process. *See generally id.* col. 5 ll. 35–64. According to the specification, clock generator 62 divides the signal from oscillator OSC to create bit-rate clock signal BCLK. Clock generator 62 feeds signal BCLK into codec 30, which converts input signal 31 into input stream 33. Input stream 33 is further converted into digital input stream SX. Clock generator 62 also forms control signal SEL, used by data selector 50. Using control signal SEL, data selector 50 “samples” bits from (i.e., selects between) user input stream 24 and input stream SX, storing the data in a single output signal RXD*—thereby synchronizing the two data streams.

II

On February 8, 2017, GET filed a complaint against Sony, alleging that Sony directly and indirectly infringes the Asserted Claims via the Accused Products. For the “encoding means” limitations, GET alleged that the Bluetooth module within the Accused Products synchronized user input from controller buttons with input from controller sensors (e.g., accelerometers).

In a March 9, 2020 *Markman* order, the district court construed the “encoding means” limitations as means-plus-function limitations. *Genuine Enabling Tech., LLC v. Sony Corp.*, No. CV 17-135, 2020 WL 1140910, at *14, *20–21 (D. Del. Mar. 9, 2020) (*Markman Order*). The court did so because the claim terms “encoding means” and “framer” failed to sufficiently denote structure to a skilled artisan, and thus 35 U.S.C. § 112(f) applied. *Id.* The court construed the “encoding means” limitations’ function as “[s]ynchronizing the user input stream with the input stream and encoding the user input stream and the input stream

into a combined data stream.” And it construed the corresponding structure as “[t]he logic design at block 34 in Figure 4A and equivalents thereof.” *Id.* No party ever suggested that the corresponding structure should be only some portion of block 34.

On the final day of fact discovery, January 22, 2021, GET served subpoenas on three of Sony’s manufacturing partners, seeking discovery on the internal structure of the Bluetooth module in the Accused Products. *See* J.A. 1459; *see also* J.A. 43. The district court denied GET’s request to extend the close of fact discovery, *see* J.A. 3212, and thus GET and Dr. Fernald never analyzed a schematic of the Bluetooth module.

At the end of discovery, the parties filed competing *Daubert* motions, and the district court excluded Dr. Fernald’s “ultimate conclusion that Block 34 of Figure 4A and the accused Bluetooth modules meet the function-way-result test for structural equivalency.” *Daubert Order*, 2022 WL 17325656, at *8. Omitting the other elements in logic block 34, Dr. Fernald’s expert report identified only the data selector, codec,⁴ and bit-rate clock as the elements involved in performing the claimed function.⁵ *Id.* at *3 (citing J.A. 1605 at ¶¶ 125–26 & 126 n.39). However, at the *Daubert* hearing, GET argued that Dr. Fernald’s position was that the “way” the “encoding means” structure

⁴ While codec 30 is not within logic block 34, the specification and testimony from Dr. Fernald demonstrate that logic block 34 synchronizes input stream 33 to the bit-rate clock by “feeding [bit-rate clock signal] BCLK to the codec, causing its output stream to clock on rising edges of BCLK.” J.A. 1605 ¶ 126 n.39; *see also* ’730 patent col. 5 ll. 10–11, 33–35.

⁵ Dr. Fernald’s expert report identified no additional elements in logic block 34 for the “encoding” portion of the claimed function. *See* J.A. 1591 ¶ 102; J.A. 1598–99 ¶ 114.

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synchronized the two streams was by “synchroniz[ing] each of the bits of the input stream and user input stream . . . to the rising edge of the [bit-rate] clock,” effectively dropping each component in block 34 except for the BCLK signal. *Id.* at *4. This narrow focus on just the bit-rate clock signal BCLK from block 34 enabled Dr. Fernald to argue that the claimed and accused structures were equivalent without ever viewing a Bluetooth module schematic. *See id.* at *5.

The court stated that while it was permissible for the “way” a structure operates to be framed at a high level, the proposition needed factual support. *Id.* at *7. The court faulted Dr. Fernald’s position as lacking discussion about what level of generality was appropriate to assess the “way” block 34 synchronized the data, or whether the elements he had previously identified, such as the data selector and codec, were sufficiently insubstantial as to be omitted from the “way.” *Id.* at *8. Because Dr. Fernald’s testimony that the claimed and accused structures were equivalent was unsupported by his limited analysis of solely the bit-rate clocks, the district court excluded his “ultimate conclusion.” *Id.*

GET filed a motion for reargument of the *Daubert* motion. *Genuine Enabling Tech. LLC v. Sony Corp.*, No. 17-CV-135, 2023 WL 4686024, at *1 (D. Del. July 20, 2023) (*Reargument Order*). In denying the motion, the court found that Dr. Fernald still failed to explain why the omitted parts of block 34 from his “way” analysis were “insubstantial” or why his simplified description of the “way” matched the specificity of the ’730 patent’s disclosure. *Id.* at *6.

A summary judgment motion followed. And, in a March 25, 2024 opinion, the district court granted Sony summary judgment of noninfringement. *Decision*, 2024 WL 1255513, at *1. The court determined that “the same principles that warranted the partial exclusion of Dr. Fernald’s equivalency analysis compel the conclusion that

[GET] lacks sufficient evidence to prove that block 34 and the accused Bluetooth module synchronize signals in substantially the same ‘way.’” *Id.* at *5.

GET timely appealed. We have jurisdiction under 28 U.S.C. § 1295(a)(1).

STANDARD OF REVIEW

This court reviews decisions on motion for summary judgment under the law of the regional circuit, which in the Third Circuit is de novo. *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1164 (Fed. Cir. 2015) (citing *Gonzalez v. Sec’y of Dep’t of Homeland Sec.*, 678 F.3d 254, 257 (3d Cir. 2012)). “[I]f the movant shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law,” summary judgment is proper. *Traxcell Techs., LLC v. Sprint Commc’ns Co.*, 15 F.4th 1121, 1127 (Fed. Cir. 2021) (quoting FED. R. CIV. P. 56(a)).

The movant “always bears the initial responsibility of informing the district court of the basis for its motion, and identifying those portions of [the record] . . . which it believes demonstrate the absence of a genuine issue of material fact.” *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986). On an issue where the nonmoving party bears the burden of proof, “[a] movant may prevail by pointing out the absence of evidence to support the nonmoving party’s case.” *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1389 (Fed. Cir. 1992) (citing *Celotex*, 477 U.S. at 325).

Though we “view all evidence in the light most favorable to the nonmoving party and draw all reasonable inferences in that party’s favor,” the nonmoving party cannot defeat summary judgment “with conclusory allegations, unsupported assertions, or only a scintilla of evidence.” *Traxcell Techs.*, 15 F.4th at 1127–28 (internal citations removed).

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DISCUSSION

I

GET appeals the district court’s determination that it failed to make a showing that the claimed and accused structures are structurally equivalent. The parties agree that “encoding means” is a means-plus-function claim limitation.

“A means-plus-function limitation recites a function to be performed rather than definite structure or materials for performing that function. Such a limitation must be construed to cover the corresponding structure . . . described in the specification and equivalents thereof.” *Lockheed Martin Corp. v. Space Sys./Loral, Inc.*, 324 F.3d 1308, 1318 (Fed. Cir. 2003) (internal citations removed). “The duty of a patentee to clearly link or associate structure with the claimed function is the quid pro quo for allowing the patentee to express the claim in terms of function under section [112(f)].” *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1211 (Fed. Cir. 2003).

“Literal infringement of a [means-plus-function] limitation requires that the relevant structure in the accused device perform the identical function recited in the claim and be identical or equivalent to the corresponding structure in the specification.” *Odetics, Inc. v. Storage Tech. Corp.*, 185 F.3d 1259, 1267 (Fed. Cir. 1999). “Once the relevant structure in the accused device has been identified, a party may prove it is equivalent to the disclosed structure by showing that the two perform the identical function in substantially the same way, with substantially the same result.” *Traxcell Techs.*, 15 F.4th at 1128 (internal citation removed). This is called the “function-way-result test” for structural equivalence of a means-plus-function limitation. *Id.*

Determination of structural equivalence does not require a component-by-component analysis. *Odetics*, 185

F.3d at 1267–68. Instead, “[t]he appropriate degree of specificity is provided by the statute itself; the *relevant structure* is that which ‘corresponds’ to the claimed function. . . . Further deconstruction or parsing is incorrect.” *Id.* at 1268 (emphasis added).

GET argues Dr. Fernald’s testimony about the “way” the structures in the ’730 patent and the Bluetooth modules of the Accused Products synchronize data streams demonstrates structural equivalence. Appellant Br. 56–61. GET attempts to recast Dr. Fernald’s analysis of logic block 34, arguing that, though the ’730 patent contains an extensive disclosure relating to FIG. 4A, very little relates to synchronization.

GET’s infringement analysis failed to meet its burden in describing the “way” the “encoding means” structure in the ’730 patent performs its function. The district court identified logic block 34 as the structure for the ’730 patent’s “encoding means,” a decision which GET did not dispute below and does not attempt to relitigate here. *See generally* Appellant Br. As discussed above, block 34 contains many different elements, but GET and Dr. Fernald’s analysis ignored most of those elements without any substantive explanation for why that was appropriate. Moreover, Dr. Fernald provided inconsistent testimony as to which subset of elements matter to the structural equivalence analysis. GET’s post-hoc attorney argument cannot fill these gaps in Dr. Fernald’s analysis.

Dr. Fernald’s expert report originally described the “way” logic block 34 performs the function of synchronization at a fairly detailed level. He highlighted portions of the ’730 patent’s specification to explain that (1) the codec uses BCLK to generate the input stream and (2) the data selector “samples” both the user-input stream and input stream on the rising edge of BCLK to create the synchronized output. *See* J.A. 1605 ¶ 126 n.39 (citing ’730 patent col. 5 ll. 33–35); *id.* ¶ 125 (citing ’730 patent col. 5 ll. 47–

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50). He reiterated in his declaration attached to GET's motion for reargument that the data selector and codec "play roles in the synchronization of the user input stream and the input stream as described in the '730 Patent." J.A. 1806–07 ¶ 9.

However, in the *Daubert* hearing, GET pared down Dr. Fernald's description of the "way," describing the role of the bit-rate clock and nothing else. *See Daubert Order*, 2022 WL 17325656, at *4. In his declaration attached to GET's motion for reargument, Dr. Fernald also reasserted his new position that the "way" block 34 synchronized the two data streams is by "synchronizing both to a common bit-rate clock." *Decision*, 2024 WL 1255513, at *3.

Despite these shifting positions, Dr. Fernald offers no meaningful explanation of why the bit-rate clock is the only part of logic block 34 that matters. GET does not argue now, nor did it attempt to argue before the district court, that the other elements of logic block 34 are, e.g., devoted to only the encoding function and therefore may be ignored for the purposes of synchronization. Thus, the district court found that Dr. Fernald was deficient in his explanation of why he had considerably curbed his analysis of logic block 34 to just one of its elements. *See Decision*, 2024 WL 1255513, at *3. We agree.

In *Traxcell Technologies*, we held that a patent owner had failed to meet its burden to show structural equivalence of a means-plus-function limitation when its expert "neglected to address a significant fraction" of a "very detailed' algorithm" identified in the patent specification as the corresponding structure. *Traxcell Techs.*, 15 F.4th at 1129. In doing so, the expert improperly "focus[ed] on function and results but elid[ed] the way those results are achieved." *Id.* We upheld the district court's determination that the patent owner did not "provide enough evidence for a reasonable jury to conclude that the accused structure performs the claimed function in 'substantially

the same way’ as the disclosed structure.” *Id.* (internal citation removed). We for that reason affirmed summary judgment of no infringement.

Here, we have a similarly detailed circuit in logic block 34, containing various signal paths and elements analogous to the algorithm in *Traxcell Technologies*. *See id.* Yet, Dr. Fernald’s analysis of the “way” logic block 34 synchronizes the two streams relies solely on the bit-rate clock. Like the expert in *Traxcell Technologies*, Dr. Fernald has “neglected to address a significant fraction” of logic block 34. 15 F.4th at 1129. Moreover, Dr. Fernald has suggested at various points in GET’s filings that the data selector and codec “play roles” in the synchronization process. *See, e.g.*, J.A. 1806–07 ¶ 9. Without further explanation of why, at least, these two elements of the structure may be ignored, GET fails to present enough evidence for a reasonable jury to conclude that the accused structure and logic block 34 are structural equivalents.

Our decision in *Dawn Equipment Co. v. Kentucky Farms Inc.*, 140 F.3d 1009 (Fed. Cir. 1998) also supports the district court’s analysis. We note that though *Dawn* is a doctrine of equivalents case, the “‘way’ and ‘result’ prongs are the same” for both literal infringement of a means-plus-function and doctrine of equivalents. *Kemco Sales, Inc. v. Control Papers Co.*, 208 F.3d 1352, 1364 (Fed. Cir. 2000). In *Dawn*, the structure of the means-plus-function limitation claim was construed as “the rotatable shaft 52, the pin 54, and the slot 72” depicted in FIGs. 1 and 2 of the asserted patent, and the accused structure consisted of a movable pin and holes to affix the pin. 140 F.3d at 1015; *id.* at 1013–14.

We remarked that, though the patent owner “presented substantial expert testimony on infringement, the experts, in testifying with regard to these two mechanisms, merely compared the pins in the two mechanisms” and made no reference to the rotatable shaft or the slot. *Id.* at

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1017. We concluded that “[m]ere comparison of the pins [was] insufficient to establish that the devices operate in substantially the same way,” because the “relevant structure disclosed in the [asserted patent] included at least the rotatable shaft, pin and slot—not merely a pin.” *Id.*

Dr. Fernald’s testimony regarding the bit-rate clock suffers from a similar issue. Logic block 34, the relevant structure, consists of several elements—some identified by GET as part of *how* block 34 synchronizes the two streams—that are absent from his description of the “way” the structure functions. *See* J.A. 1806–07 ¶ 9. Like the expert’s incomplete, pin-only analysis in *Dawn*, merely comparing the bit-rate clock of the “encoding means” structure, as GET attempts to do here, is insufficient to demonstrate that the claimed and accused *structures* are equivalent. *See Dawn*, 140 F.3d at 1017.

GET argues that the district court incorrectly required Dr. Fernald to perform the type of component-by-component analysis which this Court has deemed unnecessary to demonstrate structural equivalence. *See* Appellant Br. 52–56 (citing *Odetics*, 185 F.3d at 1268). This argument is unavailing.

First, in its denial of the reargument motion, the district court explicitly noted that it did *not* conduct a component-by-component analysis; instead, the district court faulted GET, like we do today, for its lack of explanation regarding its omissions of a significant fraction of the block 34 structure. *See Reargument Order*, 2023 WL 4686024, at *8.

Second, though we articulated a component-by-component analysis was unnecessary in *Odetics*, the patentee must still account for each element of the claimed structure in its equivalence analysis. *See Odetics*, 185 F.3d at 1264, 1269–70 (discussing the patentee’s “theory of equivalence” which focused on how the claimed structure’s rotation of “the rod, gear, and rotary loading and loading mechanisms”

compared to the rotation in the accused “bin array” structure). As *Odetics* and our caselaw demonstrate, each element of the identified structure in the specification does not need its own equivalence mapping to a respective element in the accused product. See, e.g., *Caterpillar Inc. v. Deere & Co.*, 224 F.3d 1374, 1380 (Fed. Cir. 2000) (holding the district court erred when it found no structural equivalence because the accused products “lacked a front axle, a spherical bearing, and angled struts” but had not compared “the overall structure”). But where the patentee elects to focus its equivalence analysis on something less than the whole structure that is disclosed in the specification, the patentee has an obligation to meaningfully explain why it is permissible to discard the other elements. GET failed to do so here.

Though “[o]ur case law allows for greater weight to be given to individual components that play a central role in the identified structure,” *Solomon Techs., Inc. v. Int’l Trade Comm’n*, 524 F.3d 1310, 1317 (Fed. Cir. 2008) (citing *Toro Co. v. Deere & Co.*, 355 F.3d 1313, 1324 (Fed. Cir. 2004)), this does not excuse the patentee’s obligation to account for all the elements of that identified structure and make the case for why certain elements are more central to the infringement analysis than others. In this case, GET never supplied any evidence for why many elements of its identified structure should be treated as having little to no weight in the infringement analysis.

II

While we base our decision on GET’s incomplete analysis of the identified structure in the ’730 patent, we note that GET and Dr. Fernald’s analysis of the Bluetooth modules in the Accused Products was even more sparse. See *Decision*, 2024 WL 1255513, at *5 (stating that GET offered “essentially no information regarding how the accused Bluetooth module operates” other than the involvement of a bit-rate clock). Dr. Fernald first inferred, based on

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knowledge of Bluetooth protocol, that the Accused Products' Bluetooth module synchronizes input streams from the Accused Products using a bit-clock. *See* J.A. 1606 ¶ 129. Dr. Fernald then posited that structural equivalence in logic design circuits “relies on a comparison of the operation performed . . . rather than a gate-by-gate and connection-by-connection comparison.” *Daubert Order*, 2022 WL 17325656, at *5 (emphasis added). Effectively he argues that because both structures synchronize streams to a bit-rate clock, and all logic designs performing this operation are structurally equivalent, the structure in the Accused Products, whatever they may be, must be equivalent to the patent's identified structure. Driving this very broad infringement theory was GET's failure to review schematics of the Accused Products' Bluetooth module, causing the Accused Products to be left as something of a black box.

We detect no error in the district court's rejection of this testimony. First, we agree with the district court that this testimony is conclusory. *See Daubert Order*, 2022 WL 17325656, at *5–6. GET and Dr. Fernald use the theory to bridge the gap between the “black box” accused structure and logic block 34, but a party cannot defeat summary judgment “with conclusory allegations, unsupported assertions, or only a scintilla of evidence.” *Traxcell Techs.*, 15 F.4th at 1128 (internal citations removed). Second, as the district court noted, the suggestion that an, essentially, infinite number of “ways” to accomplish a function are equivalent collapses the function-way-result test into a function-result test—an outcome that would clash with our precedent. *See Reargument Order*, 2023 WL 4686024, at *8. And finally, this argument is inconsistent with the patent's specification, which reveals a detailed logic circuit for performing the claimed function, and its prosecution history, in which the inventor stressed the claimed invention's synchronization scheme was “unique and novel.” *See* '730 patent FIG. 4A; *Markman Order*, 2020 WL 1140910, at *13.

CONCLUSION

We have reviewed GET's remaining arguments⁶ and find them unpersuasive. For the foregoing reasons, we *af-firm* the district court's summary judgment grant.

AFFIRMED

⁶ GET also appeals the district court's exclusion of Dr. Fernald's ultimate conclusion. *See* Appellant Br. 61. Because the "same principles" which led to the district court's exclusion of Dr. Fernald's conclusion also "compel[led]" the district court to grant summary judgment, we need not separately address this argument. *See Decision*, 2024 WL 1255513, at *5.